Samuel Coward

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Research Interests

Computer Arithmetic Electronic Design Automation Programming Languages Formal Verification

Education

04/21 – present **Ph.D., Imperial College London** Electrical and Electronic Engineering
Thesis title: *Equality Saturation for Hardware Synthesis and Verification.*
Supervisor: *Professor George A. Constantinides.*
Departmental Award for most promising doctoral work with 9 publications.

10/18 – 08/19 **M.Phil. Uni. of Cambridge, Distinction** in Scientific Computing.
Thesis title: *GPU-accelerated interpolation for initialising transition state searches.*

10/15 – 06/18 **BA. Uni. of Cambridge, 1st-class** in Mathematics.
College Award for academic excellence and contributions to College.

Industrial Experience

04/21 – present **Hardware Engineer** Numerical Hardware Group, Intel Corporation
Arithmetic circuit design for Intel GPUs across compute & graphics.
Supervised three interns - each leading to publication (see 1, 7 and 8 below).

11/19 – 04/21 **Firmware Engineer** Alcatel IP Networks, Nokia
Developed C++ firmware and worked on bring-up of next generation silicon.

06/17 – 09/19 **Summer Internships** Cadence (2017), Riverlane Quantum (2018) and Intel (2019)

Research Publications and Patents

Journal Articles

1. **S. Coward**, T. Drane, and G. A. Constantinides, "Localizing Constraint-Aware Optimization for Hardware Performance Optimization," ***IEEE TCAD***, 2024, [**Under Review**].
2. **S. Coward**, T. Drane, and G. A. Constantinides, "ROVER: RTL Optimization via Verified E-Graph Rewriting," ***IEEE TCAD***, 2024. DOI: 10.1109/TCAD.2024.3410154.
3. **S. Coward**, L. Paulson, *et al.*, "Formal verification of transcendental fixed- and floating-point algorithms using an automatic theorem prover," ***ACM FAC***, 2022. DOI: 10.1145/3543670.

Conference Proceedings

1. J. Cheng, **S. Coward**, *et al.*, "SEER: Super-Optimization Explorer for HLS using E-graph Rewriting with MLIR," in ***ASPLOS***, ACM, [**Best Paper Candidate**], Apr. 2024. DOI: 10.1145/3620665.3640392.
2. T. Drane, **S. Coward**, M. Temel, and J. Leslie-Hurd, "On the systematic creation of faithfully rounded commutative truncated booth multipliers," in ***ARITH***, IEEE, Jun. 2024.
3. **S. Coward**, T. Drane, E. Morini, and G. Constantinides, "Combining power and arithmetic optimization via datapath rewriting," in ***ARITH***, IEEE, [**Best Paper Candidate**], Jun. 2024.
4. B. Orloski, **S. Coward**, and T. Drane, "Automatic generation of complete polynomial interpolation design space for hardware architectures," in ***ASP-DAC***, Jan. 2023. DOI: 10.1145/3566097.3567840.

5. **S. Coward**, G. A. Constantinides, and T. Drane, "Automating constraint-aware datapath optimization using e-graphs," in ***DAC***, Jun. 2023. DOI: 10.1109/DAC56929.2023.10247797.
6. **S. Coward**, G. A. Constantinides, and T. Drane, "Combining e-graphs with abstract interpretation," in ***SOAP***, ACM, Jun. 2023. DOI: 10.1145/3589250.3596144.
7. **S. Coward**, E. Morini, B. Tan, T. Drane, and G. Constantinides, "Datapath verification via word-level e-graph rewriting," in ***FMCAD***, Oct. 2023. DOI: 10.34727/2023/isbn.978-3-85448-060-0_17.
8. A. Wanna, **S. Coward**, T. Drane, G. A. Constantinides, and M. D. Ercegovac, "Multiplier optimization via e-graph rewriting," in ***Asilomar***, IEEE, Dec. 2023. DOI: 10.1109/IEEECONF59524.2023.10476812.
9. O. Flatt, **S. Coward**, M. Willsey, Z. Tatlock, and P. Panchekha, "Small Proofs from Congruence Closure," in ***FMCAD***, Oct. 2022. DOI: 10.34727/2022/isbn.978-3-85448-053-2-13.
10. **S. Coward**, G. A. Constantinides, and T. Drane, "Automatic datapath optimization using e-graphs," in ***ARITH***, IEEE, [**Best Paper Candidate**], Sep. 2022, pp. 43–50. DOI: 10.1109/ARITH54963.2022.00016.
11. **S. Coward**, T. Drane, and Y. Harel, "Automatic design space exploration for an error tolerant application," in ***ARITH***, IEEE, Jun. 2020. DOI: 10.1109/ARITH48897.2020.00025.

Patents

1. J. Cheng, **S. Coward**, L. Chelini, R. Barbalho, and T. Drane, *Program analysis, design space exploration and verification for high-level synthesis via e-graph rewriting*, US Patent App. 18/396,321, Apr. 2024.
2. J. Cheng, **S. Coward**, L. Chelini, R. Barbalho, and T. Drane, *Super-optimization explorer using e-graph rewriting for high-level synthesis*, US Patent App. 18/396,335, Apr. 2024.
3. T. Drane, E. Morini, J. Schmerge, and **S. Coward**, *Automatic code generation of optimized RTL via redundant code removal*, US Patent App. 18/512,518, Mar. 2024.
4. T. Drane, **S. Coward**, and G. Constantinides, *Apparatus, device, method and computer program for generating an RTL representation of a circuit*, US Patent App. 18/391,716, May 2024.
5. **S. Coward**, T. Drane, and G. A. Constantinides, *Automated detection of case-splitting opportunities in RTL*, US Patent App. 18/395,066, Apr. 2024.
6. **S. Coward**, T. Drane, and G. A. Constantinides, *Hardware power optimization via e-graph based automatic RTL exploration*, US Patent App. 18/538,104, Apr. 2024.
7. **S. Coward**, T. Drane, G. A. Constantinides, and E. Morini, *Constructing hierarchical clock gating architectures via rewriting*, US Patent App. 18/538,116, Apr. 2024.
8. T. Drane, **S. Coward**, and G. Constantinides, *Apparatus, device, method, and computer program for generating a register transfer level representation of a circuit*, US Patent App. 17/649,937, Nov. 2022.
9. **S. Coward**, M. Langenbuch, and J. H. Lee, *Apparatus, device, method and computer program for an integrated development environment*, US Patent App. 17/644,112, Nov. 2022.

Awards and Achievements

2024 **Stylianos Kalaitzis Award**, Imperial College EEE, most promising doctoral work.

2022–2024 **Best Paper Candidates**, 1 × ASPLOS and 2 × ARITH.

2018 **Tallow Chandlers Award**, Selwyn College Cambridge, academic excellence.

Academic and Departmental Service

2023–present — **CAS Representative**. Represented Research Group on Post Graduate Committee. Reformed group meetings to foster collaboration and inclusive environment. Collaborated with department management on office and social space renovation.

2024–present — **Steering Committee Member**. EGRAPHS Community. Organise monthly seminar series and annual workshop.

Reviewer. Transactions on Computer Aided Design.

2023–2024 — **Program Committee Member**. LATTE and EGRAPHS Workshops.

Outreach

2021–present — **High School Project Supervision**. Four cohorts of three students across Imperial College London Maths School and Folsom Preceptorship Program (California).

2023–present — **STEM Ambassadors**. Supported school science week and school careers fairs.

Technical Skills

Coding — Verilog, Rust, C++, Linux, Git.

Tools — Logic synthesis (Design Compiler), formal verification (Jasper & VC Formal).

Technologies — Equality Saturation, SMT, Constraint Solvers, Linear Programming.

References

Professor Zach Tatlock, University of Washington, email: ztatlockcs@washington.edu

Professor Zhiru Zhang, Cornell University, email: zhiruz@cornell.edu